AMENDMENTS TO THE SPECIFICATION

Kindly delete page 1, line 19 in its entirety and substitute the following therefor:

A1

FIELD OF THE INVENTION

Please delete page 2, line 3 in its entirety and substitute the following therefor:

A2

BACKGROUND OF THE INVENTION

Please delete page 11, line 7 in its entirety and substitute the following therefor:

A3

BRIEF DESCRIPTION OF THE DRAWINGS

Kindly delete page 13, line 5 in its entirety and substitute the following therefor:

A4

DETAILED DESCRIPTION

Kindly amend the section entitled CROSS REFERENCE TO RELATED APPLICATIONS as follows:

A5

CROSS REFERENCE TO RELATED APPLICATIONS

This application is related to U.S. Patent Application Serial No. 09/753239 (~~MIPS:0104.00US~~Docket: MIPS.0104-00US) entitled "COPROCESSOR INTERFACE TRANSFERRING MULTIPLE INSTRUCTIONS SIMULTANEOUSLY ALONG WITH ISSUE PATH DESIGNATION AND/OR ISSUE ORDER DESIGNATION FOR THE INSTRUCTIONS~~INSTRUCTION ISSUE GROUPS IN A COPROCESSOR INTERFACE~~"; U.S. Patent Application Serial No. 09/751748 (~~MIPS:01075.00US~~Docket: MIPS.0107-00US) entitled "HIGHLY CONFIGURABLE CO-PROCESSOR INTERFACE"; and U.S. Patent Application Serial No. 09/751746 (~~MIPS:0108.00US~~Docket: MIPS.0108-00US) entitled "A COPROCESSOR INTERFACE ENABLING COPROCESSOR-SPECIFIC BRANCHING"; each of which are incorporated herein by reference for all purposes.

Please amend the sentence beginning on page 38, line 22 as follows:

A6

Referring to Figure 8, a timing diagram 800 is shown illustrating data transferred from the CPU 702 to the coprocessor 710 via the coprocessor interface 712 of the present invention.

Kindly amend the section entitled SUMMARY as follows:

A7

SUMMARY OF THE INVENTION

The present invention provides a scalable and configurable coprocessor interface that distinguishes between instruction types that are transferred between a central processing unit (CPU) and a coprocessor. The configurable coprocessor interface also allows sequential or parallel transfer of differing instruction types to one or more coprocessor pipelines. In addition, the interface provides separate TO/FROM data buses between the CPU and the coprocessor to allow for simultaneous data transfer (in/out) between the CPU and the coprocessor. Furthermore, the interface provides for disassociation between instructions that are transferred, and data that is transferred, to allow data elements to be moved in variable time slots with respect to their associated instructions. Moreover, the interface allows for out-of-order data elements to be transferred between the CPU and its coprocessors in an order that is not tied to the order that associated instructions are transferred (i.e., out-of-order data transfer). Out-of-order data transfer according to the present invention does not require order tags to be associated with each data transfer. Rather, the interface keeps track of the relative order of outstanding instructions that require data for execution, and provides a relative order indicator along with each piece of data as it is transferred. In addition, condition code signaling is provided from the coprocessor to allow the coprocessor to evaluate CPU specific conditional instructions, and to inform the CPU as to whether or not it should execute the CPU conditional instructions.

An embodiment of the present invention provides an interface for transferring data between a central processing unit (CPU) and a plurality of coprocessors. The interface includes an instruction bus and a data bus. The instruction bus transfers instructions to the plurality of coprocessors in an instruction transfer order, where particular instructions direct designated ones of the plurality of coprocessors to transfer the data to/from the

CPU. The data bus is coupled to the instruction bus. The data bus subsequently transfers the data, where data order signals within the data bus prescribe a data transfer order that differs from the instruction transfer order, and where the data order signals prescribe transfer of a data element corresponding to a specific outstanding instruction relative to all outstanding instructions.

A7

In another aspect, the present invention provides a computer program product for use with a computing device, the computer program product has a computer usable medium that includes computer readable program code embodied thereon. The computer readable program code causes a coprocessor interface to be described that transfers data between CPU and a plurality of coprocessors. The computer readable program code has first program code and second program code. The first program code provides an instruction bus, where the instruction bus is configured to transfer instructions to the plurality of coprocessors in an instruction transfer order, and where particular instructions direct designated ones of the plurality of coprocessors to transfer the data to/from the CPU. The second program code provides a data bus. The data bus is configured to subsequently transfer the data, where data order signals within the data bus prescribe a data transfer order that is different from the instruction transfer order, and where the data order signals prescribe transfer of a data element corresponding to a specific outstanding instruction relative to all outstanding instructions.

In a further aspect, the present invention provides a computer data signal embodied in a transmission medium. The computer data signal has computer-readable first program code and computer-readable second program code. The computer-readable first program code provides an instruction bus for transferring instructions to a plurality of coprocessors in an instruction transfer order, where particular instructions direct particular coprocessors to transfer data to/from a CPU. The computer-readable second program code provides a data bus for subsequently transferring the data, where data order signals within the data bus prescribe a data transfer order that differs from the instruction transfer order, and where the data order signals prescribe transfer of a data element corresponding to a specific outstanding instruction relative to all outstanding instructions.